

Remarks

The examiner's reconsideration of the application is requested in view of the amendment of claim 1 above, and comments which follow.

The examiner has rejected claim 1 and dependent claims 7, 8 and 10 under 35 U.S.C. §102 as being anticipated by Chi U.S. Patent Number 5,608,243. Claims 6 and 9 have been rejected on the basis of obviousness, again with Chi being the primary reference. Reconsideration of the rejections is requested.

Claim 1 of the patent application in reference has been amended, so as to still better distinguish from Chi.

In the pixel structure according to the present invention, and as now explicitly stated in the amended set of claims annexed hereto, there are no means for storing carriers in between "the region for collecting but not storing carriers" and the "at least one planar current flow, carrier transport pathway".

In Chi on the contrary, charges are stored between the collection region and the planar pathway, more particularly in the drain region 108. See page 3, lines 57-: *"During image integration, photons strike the surface of p+region 114 and, as a result, create a number of electron-hole pairs. The photo-generated electrons are swept to the drain region 108 due to the built-in electrical field in the junction."*

At his location, i.e. at the drain region 108, the electrons are kept, or thus stored, up to the moment when the floating gate 116 is at a potential that is positive enough to generate a channel in the substrate underneath it such that carriers can flow towards the source region 106 (when a suitable voltage V_{read} is applied to the control gate). This means that, according to Chi, means (the drain region 108 in combination with the floating gate electrode 116) are provided for

storing carriers in between the region for collecting but not storing carriers (p+ region 114) and the at least one planar current flow carrier transport pathway.

This is definitely not the case in the device according to the present invention. According to the present invention, no carrier storing takes place between the image collection region and the planar current flow pathway. Carriers which are collected in the region in the substrate for collecting but not storing carriers, directly flow from or through this region over the planar current flow carrier transport pathway to the at least one doped or inverted region of a first conductivity type in or on the substrate, which region is meant to store the carriers up to the moment of readout.

The Examiner states on page 5 of the June 2, 2004 Office Action that "the charges that form the current are not stored in an intermediate location but reside in a drain region 108". The fact that they reside there means that they are stored there!

As amended claim 1 is considered to be novel and non-obvious, and thus allowable, dependent claims 6 to 10 are considered patentable as well by virtue of their dependence from claim 1.

* * *

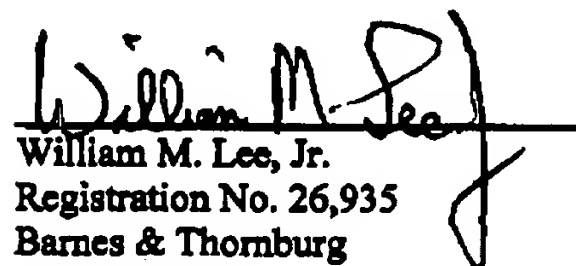
With regard to the drawing objection, it is respectfully submitted that the regions of a second conductivity type in or on the substrate avoiding touching of the region for collecting but not storing carriers, as claimed in claim 9, are illustrated as regions 15 in Fig. 10b of the drawings as presently on file.

Therefore no drawing correction is deemed to be necessary.

In view of the above, the examiner's further and favorable reconsideration of the application is urged.

September 2, 2004

Respectfully submitted,


William M. Lee, Jr.
Registration No. 26,935
Barnes & Thornburg
P.O. Box 2786
Chicago, Illinois 60690-2786
(312) 214-4800
(312) 759-5646 (fax)